PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10078340	02/21/2002	~~257~~		~~2811~~ 2823	

**APPLICANTS: Tomita Hiroyoshi;

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A DIV OF 09/587,296 06/05/2000 PAT 6,373,783

** FOREIGN APPLICATIONS VERIFIED:
JAPAN HEI 11-310036 10/29/1999

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		108397-00067
Verified and Acknowledged Examiners's intials			

TITLE : Semiconductor integrated circuit, method of controlling the same, and variable delay circuit

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING	
Amount Due	Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAIMER		Primary Examiner	Application Examiner	
		PREPARED FOR ISSUE		

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

FILED WITH: ☐ DISK (CRF) ☐ CD-ROM
(Attached in pocket on right inside flap)